ECE480 Design Team 5
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Over-Current Protection Reference Design and Study

Progress Report I

3/17/2011

Application 1- Tablet PC Over-Current Protection System

The design for this application gained momentum right from the start of the semester. The initial schematic and block diagrams were created within the first two weeks of the project. This original design can be found in the proposal. A first-run PCB was also fabricated for this original idea; however, once testing began, design issues became evident. Since these issues were discovered early, new parts were selected to optimize the design before fabricating the next PCB.

The tablet-PC over-current protection system still follows the original design from the proposal closely, however many of the parts have been replaced for various reasons. The INA138 has been replaced with the more accurate INA214, which has a 60μV offset compared to the 1mV of the INA138. The TLV3491 comparator is being replaced with the TLV3501, which is much faster, with a switching speed of 4.5ns instead of the 6μs. Finally, the voltage divider used in the original design has been replaced with the REF3025, a 2.5V voltage reference, which will make the design more reliable when working with a battery, which may have a nominal voltage of 3.6V, but supply less when used. The TPS2033 power distribution switch is currently the bottleneck in system performance, and needs a replacement part since it is very slow, running with a switching delay of about 18ms. Replacements currently being researched include the TI TPS1100/1101 power MOSFET or possibly a part from another

company, such as the Vishay Si3865BDV power distribution switch. However, the team has decided to test the updated design to verify that it works, before changing the switch to optimize the speed performance of the circuit.

The goal for completion of the final design is currently April 14, 2011. By then, a working design with optimal operation will be completed with valid test results supporting the decision. This date should provide enough time to professionally fabricate a PCB and complete the final report on this application prior to Design Day.

Application 2- Cell Phone Current Display

The design for this application took slightly longer than the first application since it includes the use of an MSP430 microcontroller. At this point, an initial block diagram has been completed as well as some early code. A PCB is also in the processing of fabrication alongside the application one PCB. The parts for this design have been selected, ordered, and received. The block diagram and part selection information is included in the final proposal.

The PCB testing for this board will only include parts up to the analog-to-digital converter to show that the digital signal is being created correctly. The MSP430 has not been included in the initial PCB design because of the added complexity of soldering the small pins would delay hardware testing. By adding breakout pins to the board, the analog-to-digital signal can be sent to TI's MSP430 experimenter board for quick and easy debugging of the software side without the need for complicated interfaces.

The goal for this final design is also April 14, 2011, again leaving enough time to professionally fabricate a final board and write a full report on this part of the project.

Studies

Studies cannot start until a working design for both applications are completed. Starting early next week, the team will decide on the topics for the studies, and what type of data will be gathered. The goal is to have at least two studies completed by April 14, 2011 in order to guarantee that there is ample data for the studies in the final report, required by Design Day.

Budget

Texas Instruments has provided most of the parts required at this time, for no cost, as samples, including analog ICs, the MSP430, and MSP430 development materials. However, current shunt resisters, along with some INA214 (on backorder), have been ordered using the team budget. In the future, the budget will be used to purchase more parts from other companies as well as any TI parts placed on backorder. A portion of the budget is currently reserved to place our final designs on professionally fabricated PCBs, which may cost $200 or more depending on which supplier is used, and PCB setups. The current budget report is as follows:

Last Name	Email Address	Date Requested	Date Complete	Shipping	Total Cost	Order Complete
Laderach	laderac1@msu.edu	2011-02-18	2011-02-28	6.10	9.91	Yes
Laderach	MSU480DT5@gmail.com	2011-03-17	0000-00-00	0.00	25.22	No

Budget = $500

Amount Spent = $35.13 Shipping total = $6.1 Amount left in Budget = $464.87

Gantt Chart

Our current (March 19, 2011) Gantt chart is appended on the following page. Note that the sub tasks for application one have been minimized, since they are similar to application two, to reduce redundant reporting. The current schedule will allow for completion of this project by Design Day.

ID	Task Name	Duration	Start	Finish
1	**ECE 480 Design Project**	**78 days**	**Fri 1/14/11**	**Mon 5/2/11**
2	**Design Team Meeting**	**73 days**	**Thu 1/20/11**	**Thu 4/28/11**
17	Initial Meeting with Sponsor	0 days	Mon 1/24/11	Mon 1/24/11
18	Six Sigma Homework	3 days	Fri 1/28/11	Mon 1/31/11
19	Preproposal	5 days	Wed 2/2/11	Mon 2/7/11
20	Initial Website Design	4 days	Tue 2/8/11	Fri 2/11/11
21	~~Meeting with Sponsor~~	~~0 days~~	~~Wed 2/2/11~~	~~Wed 2/2/11~~
22	Meeting with Sponsor	0 days	Fri 2/11/11	Fri 2/11/11
23	Part List	0 days	Tue 2/8/11	Tue 2/8/11
24	Order Parts	0 days	Mon 2/14/11	Mon 2/14/11
25	**Application One**	**61 days**	**Mon 2/7/11**	**Thu 4/28/11**
39	**Application Two**	**61 days**	**Mon 2/7/11**	**Thu 4/28/11**
40	Research App 2 (Microcontroller Operation and Initial Design Ideas)	7 days	Mon 2/14/11	Tue 2/22/11
41	Block Diagrams/Schematics	5 days	Wed 2/23/11	Tue 3/1/11
42	Initial Software	16 days	Wed 2/23/11	Tue 3/15/11
43	**Main Design**	**32 days**	**Tue 3/15/11**	**Thu 4/28/11**
49	**Studies**	**22 days**	**Wed 3/16/11**	**Thu 4/14/11**
54	Proposal Presentation	0 days	Mon 3/14/11	Mon 3/14/11
55	Progress Report #1 Due	0 days	Fri 3/18/11	Fri 3/18/11
56	**Technical Lecture**	**0 days**	**Fri 4/1/11**	**Fri 4/1/11**
59	Progress Report #2 Due	0 days	Fri 4/15/11	Fri 4/15/11
60	Complete Final Report	7 days	Fri 4/15/11	Mon 4/25/11
61	Individual Application Notes Due	0 days	Fri 4/1/11	Fri 4/1/11
62	Design Issues Paper Due	0 days	Fri 4/15/11	Fri 4/15/11
63	Professional Self Assesments Due (Individual)	0 days	Wed 4/20/11	Wed 4/20/11
64	**Design Day**	**7 days**	**Fri 4/22/11**	**Fri 4/29/11**
67	Final Submission	0 days	Mon 5/2/11	Mon 5/2/11